CpE Lab

Section 002

Lab 5: Introduction Logic Simulation

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**Introduction**

The main goal of this lab was to introduce to students a process known as logic simulation, which is used to simulate the behavior of a circuit before the final steps in the design of the circuit are taken, and to teach students how to simulate circuits using the simulation tool on Quartus II.

**Part I**

**Experiment**

This part of the lab involved designing a two way light controller consisting of two inputs and one output through the means of a VHDL program.

**Methodology**

This task was completed with little or no effort as the VHDL code for the two way light controller was already provided in the lab handout. Hence the team created a new project and copied the given code unto the VHDL editor and compiled it. Shown below is an image of the code for the light controller as it was entered in the VHDL editor.



Figure VHDL code for light controller

**Result**

The code compilation was successful

**Part II**

**Experiment**

This experiment involved the simulation of the two way light controller in order to determine if the circuit had been designed correctly and that the desired output would be obtained. The truth table was provided and can be seen below.



Figure 2 Truth table for light controller

**Methodology**

Following the instruction provided on the lab handout, the team proceeded to create the test vectors to represent the input signals of the circuit. The first step taken to achieve this was to launch the Waveform editor (the tool on Quartus II used to simulate circuits) and to save it under the name “lab5”. The desired simulation was then set to run from 0 ns to 200 ns, and the node finder was used to find the two inputs and and the output . Next the input values from truth table shown in figure 2 were represented by test vectors on the waveform editor. This was done by setting input to 0 in the 0 to 100 ns time interval and 1 in the 100 to 200 ns time interval, and input to 0 in both the 0 to 50 ns and the 150 to 200 ns interval and 1 everywhere else. After this, the file was saved and simulated.

**Result**

The truth table was verified as the resulting waveform agreed with the expected output of the circuit.

**Part III**

**Experiment** The task here was to design a 3 bit adder using VHDL and simulate it using four different input vectors. The chosen operations to be performed by the three bit adder are: 0+0, 4+4, 6+1, and 7+7, and these operations are shown below in the form of a truth table.



Figure input vectors

**Methodology**

Following the same process used in part II of this lab; the group wrote and compiled the following VHDL code for the 3 bit adder

**LIBRARY ieee;**

**USE ieee.std\_logic\_1164.all;**

**ENTITY lab4part2 IS**

**PORT (**

**X1 : IN STD\_LOGIC;**

**X2 : IN STD\_LOGIC;**

**X3 : IN STD\_LOGIC;**

**Y1 : IN STD\_LOGIC;**

**Y2 : IN STD\_LOGIC;**

**Y3 : IN STD\_LOGIC;**

**F1 : OUT STD\_LOGIC;**

**F2 : OUT STD\_LOGIC;**

**F3 : OUT STD\_LOGIC;**

**F4 : OUT STD\_LOGIC**

**);**

**END lab4part2;**

**ARCHITECTURE Behavior OF lab4part2 IS**

**SIGNAL C1 : STD\_LOGIC;**

**SIGNAL C2 : STD\_LOGIC;**

**BEGIN**

**F1 <= (X1 xor Y1);**

**C1 <= (X1 and Y1);**

**F2 <= (X2 xor Y2) xor C1;**

**C2 <= ((X2 xor Y2) and C1) or (X2 and Y2);**

**F3 <= (X3 xor Y3) xor C2;**

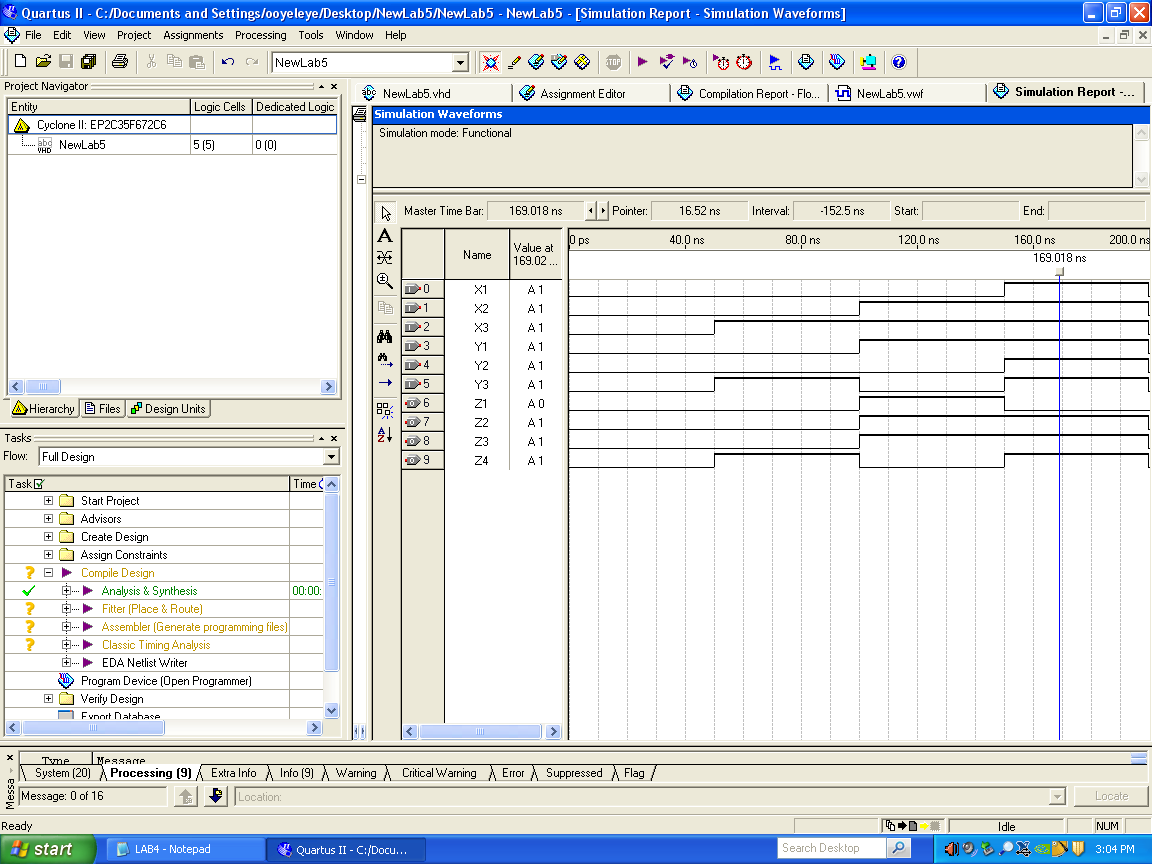
**F4 <= ((X3 xor Y3) and C2) or (X3 and Y3);**

**END Behavior;**

Just as before set the simulation to run from 0 to 200 ns. The six inputs and , and the outputs and were selected, and the various input combinations shown in figure 2 were converted into test vectors and laid unto the waveform editor. Finally the file was saved and then simulated, and the output waveform was generated.

**Result**

The simulation was a success as the expected resulting waveform was obtained. Below is a screen shot of the resulting simulation.



**Post Lab Questions for Lab 5**

The first step in the logic design flow is the concept, which is simply the desired outcome from a circuit. Next is the design entry which is simply the process of drawing the schematics for this desired circuit or coding it using VHDL. After this, the design is shaped into a circuit made up of the logic elements in the FPGA chip. Now this is where simulation comes in, and it is simply using a simulation tool to verify that the circuit design is correct. After a successful simulation, the circuit is then mapped on the desired FPGA, and the chip is then programmed.

**Pre Lab Questions for Lab 6**

|  |  |  |  |
| --- | --- | --- | --- |
| SEL2 | SEL1 | SEL0 | A/B DATA |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

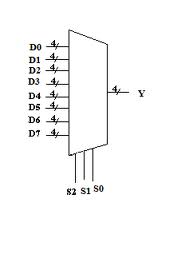


Figure 3 Black box diagram